

# Benefits of Behavioral Modeling of Analog / Mixed-Signal Subsystems using standard HDL languages

*by Dayanand Reddy, Milam Paraschou, Curt Schnarr and Mike Hegre*

In recent years there has been a significant increase in the verification complexity and effort required for integrated circuit (IC) design. Many of today's ICs employ large and complex analog or mixed-signal subsystems to perform increasingly complicated tasks. The analog/mixed-signal subsystems themselves are increasingly multidisciplinary, often involving multiple design teams using multiple design techniques. With time to market as critical as ever, and mask costs going through the roof, we need an efficient means to thoroughly verify designs containing these subsystems.

Complex mixed-signal designs present significant verification challenges. While the digital portion of ICs are efficiently verified using HDL simulators, the analog portions and their interface to the digital realm have typically had to rely on some type of "SPICE-like" or mixed-signal simulator. Use of these kinds of tools for verifying those systems can be both slow and expensive. For example, it can take a painfully long time to run SPICE analysis on high-performance circuits that employ slow feedback loops that have long time constants for conditioning the response. Spread Spectrum PLLs and Sigma-Delta converters would be examples of widely used circuits that fall into this category.

This paper will examine common simulation challenges within the subsystem architecture definition/verification and the subsystem integration tasks of complex mixed-signal designs. Then we'll look at how behavioral models employing standard HDL languages such as Verilog and VHDL can be used to efficiently and cost effectively to address those challenges.

## Subsystem Architecture Definition and Verification

Once the specification for a subsystem has been completed, an initial hardware architecture can be defined. The proposed architecture must be verified to insure that it meets design specifications. Let's look at some of the issues involved with verifying some common mixed-signal subsystems.

Serializer-Deserializers (SERDES) are very common mixed-signal subsystems within today's ICs. SERDES are used in a wide variety of applications including, but not limited to, storage and communication systems. SERDES contain Clock-Data Recovery (CDR) blocks that are used to separate the clock and data signals contained within a serialized bit-stream. These CDR blocks often employ complex architectures where it becomes difficult, if not inhibiting, to try to account for all factors during the design stage. For example, bang-bang CDR loops that employ up-down charge pumps in conjunction with an RC filter may be designed using control theory, but that theory is typically incomplete and will require simulation for completeness. Analysis of Phase Locked Loops (PLLs) and CDR loops that utilize linear charge pumps will often not account for the effects introduced by the digital sampling action of the phase detector, and thus, will also require simulation to insure design confidence. The same is true with the more DSP intensive architectures that employ digital processing of the phase detector output in order to control mixers within the loop. While the control theory behind these loops is understood, its typically not treated with as much detail as one would hope due to the complexities introduced when trying to do so. Once again, simulation needs to be relied on in order to verify correctness.

As we can see, simulation is a critical component in the verification of mixed-signal subsystems, Unfortunately, simulation of these systems is often very time consuming when using SPICE or even "fast SPICE-like" simulators. Consider for example, systems where high performance circuits are used in slow feedback loops to manipulate the circuit behavior. Some circuits that come to mind are high-

speed PLLs that are used in loops to generate a spread-spectrum clock output for reducing EMI emissions. The slow time constant required of the loop (approx. 30kHz) makes simulation of the system within a SPICE-like simulator both cumbersome and very time consuming. A similar situation exists with sigma-delta converters. While mixed-signal simulators are an option, they are relatively expensive and typically offer limited speed improvement. We need a better method to accurately and efficiently simulate these mixed-signal subsystems so that we can support both the architecture verification and the system feasibility analysis tasks.

## **Subsystem Integration**

The system integration task involves assembling the various subsystem blocks into the top-level of the IC. Prior to committing to tape-out it is imperative to verify that the interaction between the blocks is correct and that the overall functional requirements have been met. Once again, simulation typically plays a large role in this verification, and once again, mixed-signal designs present some interesting challenges.

This verification task will typically fall to the system designer or a dedicated verification engineer. Rarely, will the subsystem block designer perform the system-level verification. In fact, often times the subsystem IP is provided by third parties that the verification engineer has limited access to. The verification engineer seldom has access to the SPICE netlists/models for that third-party IP, and even if he did, using SPICE-like simulators at this level is typically so excruciatingly slow that it's completely unwieldy. If models are provided, then they're more likely to be either simple black-box verilog models, which offer limited and usually idealized circuit behavior, or occasionally, more elaborate and more comprehensive Verilog-A behavioral models. While the former simulate very quickly, they offer little in terms of design verification confidence. On the other hand, Verilog-A behavioral models can include tremendous detail and thus can provide a means to thoroughly verify mixed-signal designs. The downside is the cost of the more expensive Verilog-A capable simulators and the significantly higher simulation run times.

As an example, let's look at the SERDES again. SERDES designers are often required to design the systems with features that can support multiple standards. These systems will typically need to employ multiple configuration settings, multiple calibration settings, as well as the use of state machines in order to meet those requirements. Clearly, there needs to be a significant amount of simulation or simulation coupled with formal verification to insure that all system requirements are met. The optimal simulation solution would be a low-cost approach that could provide sufficient detail and accuracy while maintaining sufficiently high simulation throughput.

## **Benefits of Using Models that Employ Standard HDL Languages**

The need for modeling analog and mixed-signal subsystems has resulted in a number of options being made available to designers:

- General purpose simulators like Matlab can be used to simulate control loops, and to some extent, mixed-signal subsystems as well. The main drawback of using such simulators is the inability (or the complexity involved) to interact with the simulation of the digital content of the IC. It is also quite challenging to model large mixed-signal subsystems such as CDR blocks.

- Mixed-Signal HDL simulators now allow for analysis of mixed digital/analog circuits. These simulation environments must carry the burden of the compute-intensive analysis of the analog content as well as the overhead involved with the communication between the digital and analog simulation processes. This accounts for their relatively slow simulation times.

- Verilog-A, a relatively new HDL, provides a means to develop analog behavioral models. HDL

simulators that support Verilog-A offer some throughput improvements for verifying analog/mixed-signal designs, but they are still significantly slower and more costly than their strictly digital counterparts. The lower throughput becomes quite apparent when trying to simulate large blocks or entire systems.

Mixed Mode Solutions, Inc. (MMS) has developed a method whereby the real-time behavior of complex analog functions/circuits can be described with surprising accuracy using standard HDL constructs. Key circuit aspects such as digital-sampling characteristics can readily be accounted for. The circuits simulate very quickly using standard, relatively inexpensive, digital HDL simulators. There is no simulation overhead incurred due to the interaction between multiple simulators. These models can also provide for programmable speed-accuracy adjustment so that the performance can be tuned appropriately for the task at hand.

Let's look at some examples of what can be achieved with using this methodology. Behavioral models of PLLs can be implemented with relatively high accuracy. The figures below were generated using a behavioral PLL model using standard Verilog constructs. The model reproduces the behavior of a 3<sup>rd</sup> order PLL (second order loop filter). The figures below indicate the phase error and output clock frequency of a PLL model from power up to lock-in. The plot in **Figure 1** shows a 3<sup>rd</sup> order PLL loop with a phase margin of 70 degrees. The plot in **Figure 2** shows the same loop with a transport delay introduced in the feedback loop to reduce the phase margin to 30 degrees. The plot in **Figure 3** shows the same reduction in phase margin achieved by increasing the 3<sup>rd</sup> order capacitor.

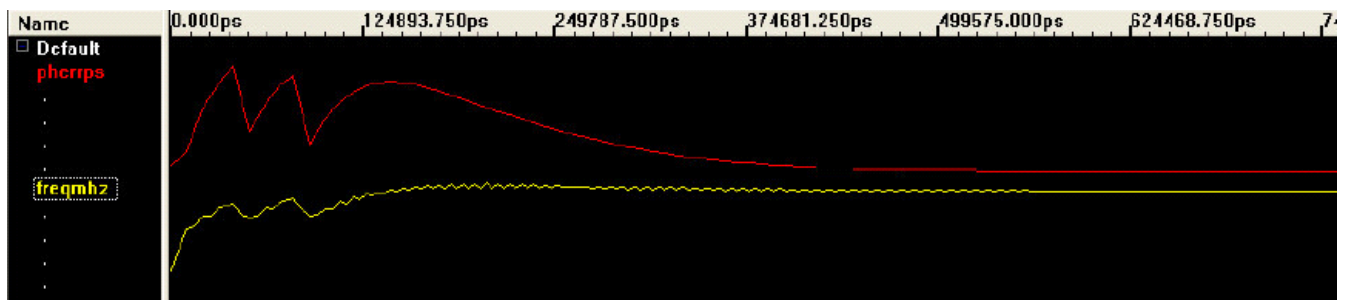


Figure 1: PLL loop response with 70 degrees Phase Margin

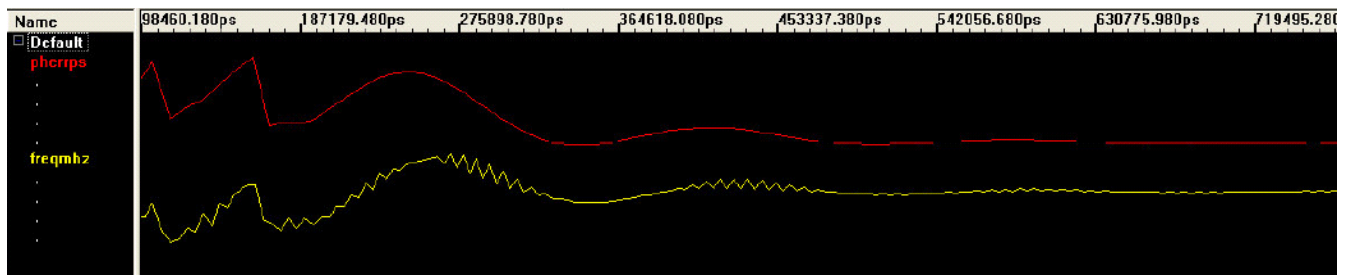


Figure 2: PLL loop response with 70 degrees Phase Margin reduced to 30 degrees by transport delay

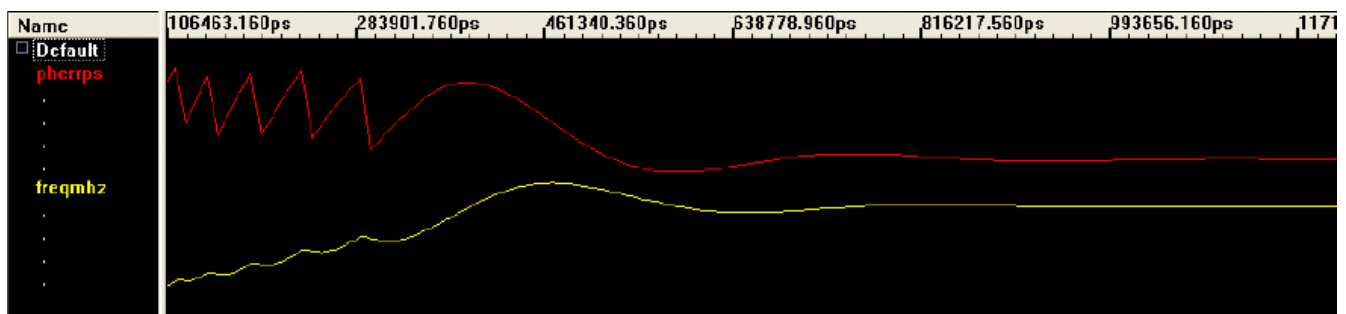
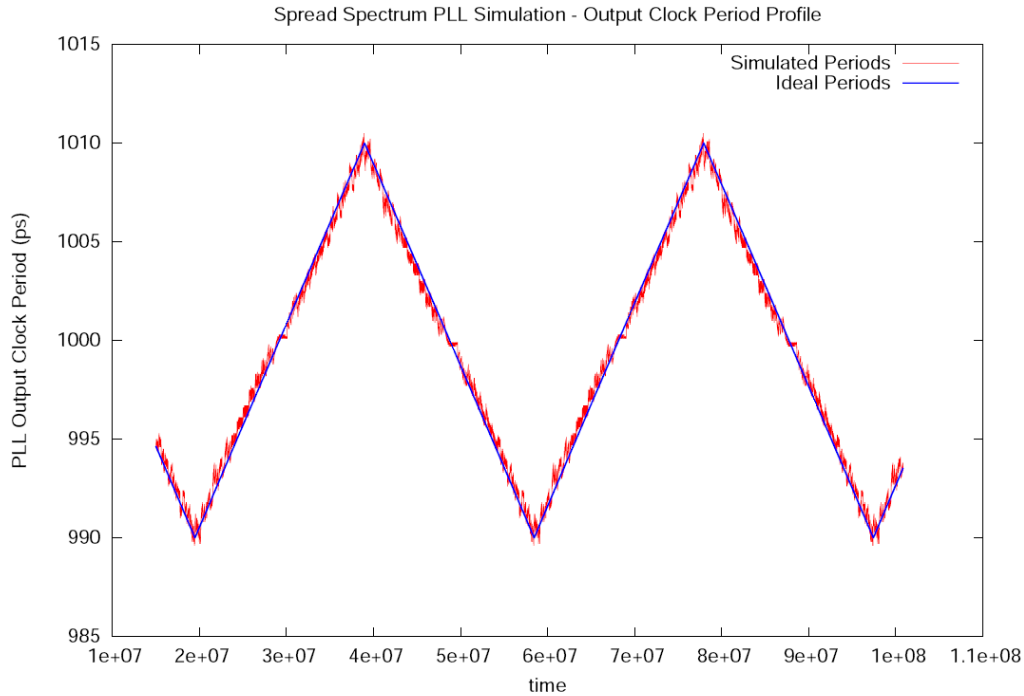


Figure 3: PLL loop response with 70 degrees Phase Margin reduced to 30 degrees by larger 3<sup>rd</sup> Order Capacitor

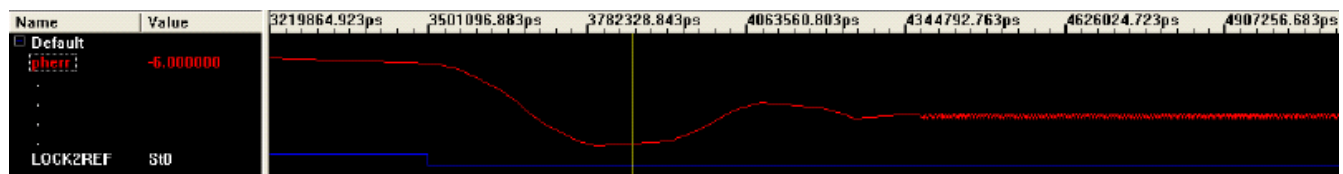
The plot in **Figure 4** shows the output clock period of a PLL used in a Spread Spectrum PLL loop. The plot shows the measured periods of the PLL output running at 1.25GHz while being modulated by 1% at a rate of 40kHz. The solid line is the idealized spread spectrum clock and the fuzzy signal is the real simulated clock output. The output clock information can be written to a file and then analyzed for spectral content information. This simulation used a 100fs resolution and required only 12mins to simulate a 100us timespan. During the initial stages of architectural development we used a resolution of 1ps and the runtime was less than 3 minutes to cover the same 100us timespan. To gather spectral content information we ran with a resolution of 1fs and these simulations were completed in 1hr 8mins. Again, we can tune the models simulation speed/accuracy to the task at hand.



**Figure 4:** Spread Spectrum PLL loop output

We have also modeled SERDES blocks using these constructs as well as architectures involving linear charge-pumps, integrating phase detectors, bang-bang phase detectors, and RC filter / VCO and VCO / interpolator combinations.

The plot in **Figure 5** shows the phase error at the sample latches for a 3 Gbps clock and data recovery block (CDR). The CDR block that is modeled uses an integrating bang-bang phase detector in conjunction with a VCO and RC filter. The phase error shown is at the point when the CDR block switches over to lock to data. The simulation was run at a 1ps resolution.



**Figure 5:** Phase Error at sample latches for a Bang-Bang CDR loop

We also modeled other circuits such as analog lock detectors with RC time constants, analog DLLs, and digital PLLs using the same techniques.

## **Conclusion**

Mixed Mode Solutions, Inc. (MMS) has developed a novel technique for providing detailed analog behavioral modeling using standard HDL constructs. This modeling technique provides for accurate and rapid verification of both analog/mixed-signal subsystem architectures as well as complete integrated systems using relatively low-cost Verilog or VHDL simulators. MMS licenses their EVAL© Family of Modeling IP and can also provide custom modeling services.

### About the authors:

Dayanand Reddy, Milam Paraschou, Curt Schnarr and Mike Hegre are principals and co-founders of Mixed Mode Solutions, Inc. ([www.mixedmode.com](http://www.mixedmode.com)).