Mixed Mode Solutions, Inc.

Product Brief
Communication and Control Models

Benefits:

- **Early Architectural Validation of Analog Performance and Digital Interfaces for Components and Subsystems with Large Time Constants**
- **Early Detection of Functional and Timing issues via Compliance Pattern Testing**
- **Ability to Reduce Analog Accuracy for Improved Digital Simulation Throughput**
- **Ability to Speed up System Verification and Validation via Co-Simulation**
- **Uses Standard Control Loop parameters**
- **Verilog – A Not Required**

Applications: Components

- **VCO's, Linear Charge Pumps, Bang-Bang Charge Pumps, RC Networks, Delay Elements, Phase Interpolator, Integrators**

Applications: Subsystems

- **PLL's, Spread Spectrum Clocking, SigmaDelta, SerDes, SATA, PHY, TIA, PCIe, Clock/Data Recovery, High Speed Interfaces and other Analog Circuits**

Description:

Mixed Mode Solutions Inc. Communication and Control models are available to support behavioral modeling of component, subsystem, and system level interactions to support verification, validation, and vector generation during all phases of the development and design process. Models are supported in Industry Standard Verilog with porting to VHDL supported upon request. Verilog – A is not required.

Uses:

Communication and Control Models are used both at the component, subsystem, and system level to verify analog performance, functional behavior, and system interaction via stand alone Verilog Test Benches and/or Co-simulation in Cadence/Hspice/SmartSpice environments.

Simulation of long time constants and closed loop systems is computationally intensive consuming critical schedule time. MMS behavioral Models reduce simulation time which allows for many test cases, vector sets and patterns to be verified, reducing silicon risk.

Models can be used to mimic behavior of complex analog sub-systems such as SATA, PCIexpress transmit/receive blocks during pattern verification allowing analog and digital sections to be verified concurrently through functional test benches and the entire system behavior validated.

Several Analog sub-systems which are difficult to model can be verified with MMS behavioral models.

- Model non-linear bang-bang loops for architectural validation.
- Model Sigma-Delta circuits to verify interaction with digital subsystems as well as architectural validation.
- Model phase locked loop behavior to verify system interaction during startup, lock-in, test/bypass states and responses to frequency steps or other complex functions which analog subsystems perform during system operations.
- Model Spread Spectrum clock generation subsystems.

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- Model SerDes blocks implemented using a variety of architectures.

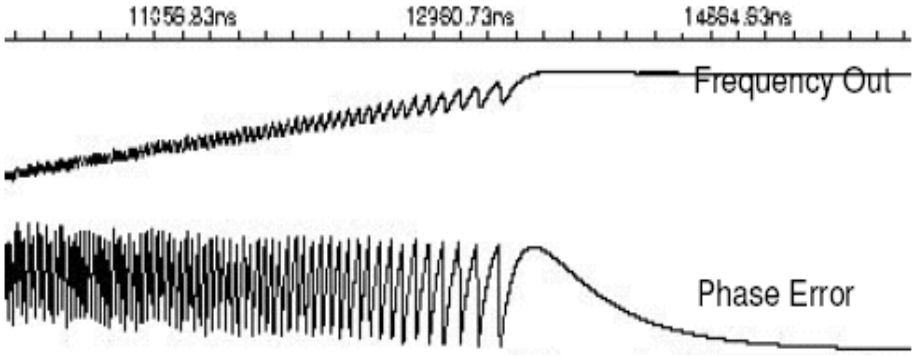

Figure 1. MMS PLL Behavioral Model during Lock-in shown below.

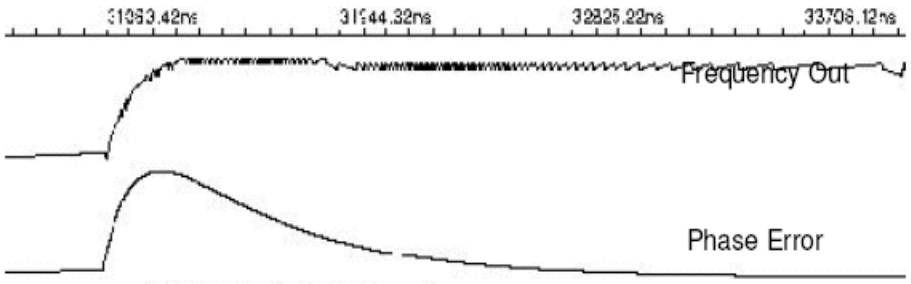

Figure 2. MMS PLL Behavioral Model during 3% frequency step shown below.

Availability and Pricing:

- Analog Component, Generic PLL, SERDES models Available.
- When customer needs exceed MMS Standard Behavioral Model capability, Custom Models and model tailoring are available on request.
- Fixed Price or Price-per-use pricing available on Standard Models.

Contact Mixed Mode Solutions with your model needs Today!:

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