Product Brief - EVAL© Behavioral Modeling IP

Benefits:

- **Quick validation of analog and digital components and subsystems**
- **Early detection of functional and timing issues via compliance pattern testing**
- **Ability to optimize analog accuracy for improved digital simulation throughput**
- **Ability to speed up system verification and validation via co-simulation**
- **Uses standard control loop parameters**
- **Verilog–A not required**

Building Blocks:

- **VCOs**
- **VCDLs**
- **Linear and Bang-Bang Phase Detectors**
- **Charge Pumps**
- **RC Filter Networks**
- **Delay Elements**
- **Phase Interpolators**
- **Arbitrary Gain and Phase Modeling Blocks**

Applications: Subsystems

- **PLLs, DLLs**
- **Spread Spectrum Clocking**
- **Sigma-Delta Converters**
- **SerDes, SATA, PHY, TIA, PCIe, and DDR3**
- **General communication interfaces and other complex time-dependent systems**

Description:

Mixed Mode Solutions Inc. Verilog behavioral models are available to support behavioral modeling of component, subsystem, and system level interactions to support verification, validation, and vector generation during all phases of the development and design process. Accurate modeling of complex analog circuits is achieved using the EVAL© (Early Validation of Architectures and Logic) set of behavioral modeling IP. Models are supported in Industry Standard Verilog with porting to VHDL supported upon request. Verilog-A is not required.

Uses:

Behavioral Models are used both at the component, subsystem, and system level to verify analog performance, functional behavior, and system interaction via standalone Verilog Test Benches and/or Co-simulation in Cadence/Hspice/SmartSpice environments.

Simulation of long time constants and closed loop systems is computationally intensive, consuming critical schedule time. MMS behavioral models reduce simulation time, which allows for many test cases, vector sets and patterns to be verified, reducing silicon risk.

The staff at MMS have extensive behavioral modeling experience. Behavioral models can be tailored to your specific needs and requirements. In addition, models can be generated to replicate complex analog circuit behavior to a very high degree of accuracy. This is achieved using the EVAL© set of behavioral modeling IP.

Use of fast, accurate models provides early validation of system architecture as well as extensive characterization coverage of systems that require long simulation times to validate system behavior. The same models can then be used to verify interaction with other Analog / Mixed-Signal subsystems and finally can be

used to verify behavior at the overall chip level. Since the same model can be used through all the stages, the probability of miscommunication between the various stages is eliminated. For most chip-level Verilog simulation

environments, runtime is not impacted noticeably. Also, in the situation where the chip contains a large number of modeled sub-systems (eg., 16 lane PCI Express transceiver chips), the resolution of the models can be reduced to improve run-times without significantly affecting accuracy.

The EVAL Models can be used to represent behavior of complex analog sub-systems such as SATA and PCIexpress transmit/receive blocks during pattern verification allowing analog and digital sections to be verified concurrently through functional test benches and the entire system behavior validated.

Figure 1. shows the Jitter Transfer Curve generated using the Phase Locked Loop (PLL) behavioral model. The model mimics the behavior of a 3rd order PLL (2nd order loop filter). The three cases analyzed are the same PLL analyzed when varying the size of the 3rd order capacitor and thereby impacting the Pole-Frequency and other loop parameters.

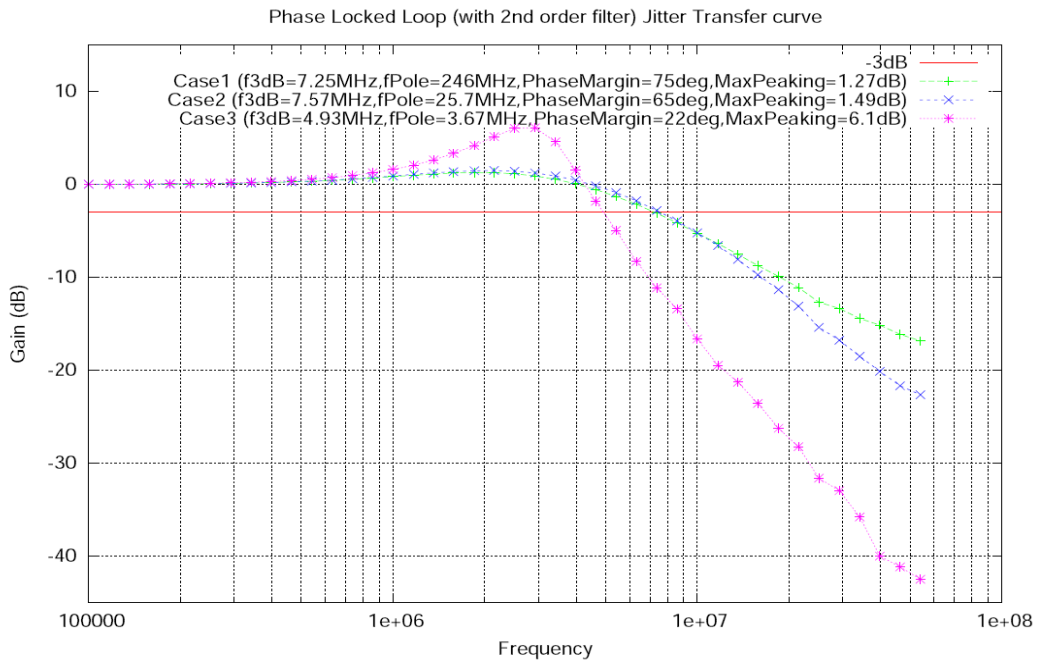

Figure 1. MMS PLL Behavioral Model Jitter Transfer Curve

Figure 2. shows shows the lock-in profile for the same cases, generated using the Phase Locked Loop (PLL) behavioral model. The model emulates the behavior of a 3rd order PLL (2nd order loop filter). The three cases analyzed are the same PLL analyzed when varying the size of the 3rd order capacitor and thereby impacting the Pole-Frequency and other loop parameters.

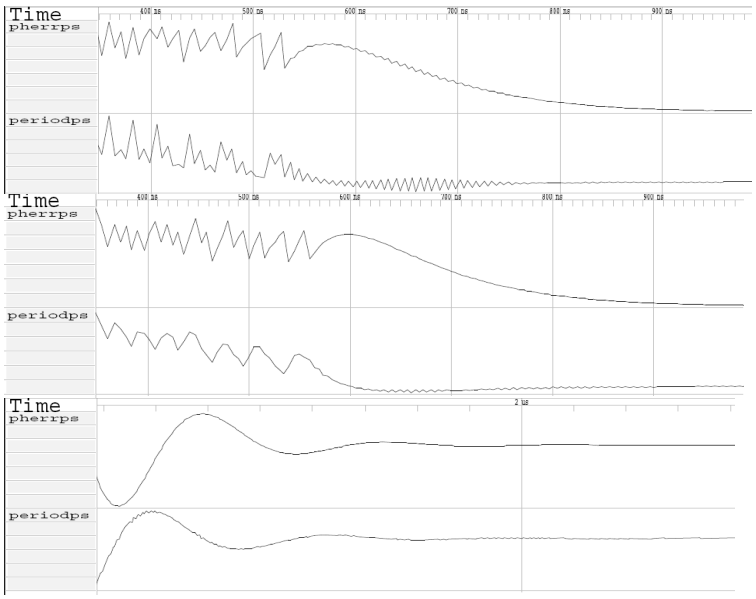

Figure 2. MMS PLL Behavioral Model Lock-In Phase Error Profiles

The ability to simulate transfer curves is especially useful in evaluating CDR blocks using Bang-Bang type phase detectors or DSP type architectures, and to evaluate situations where the input data has a particular pattern, such as PRBS data or 8b-10b data. The numerical data can be easily post-processed to infer the f3dB and peaking characteristics of the block. The 'max peaking' and 'f3dB' data shown in Figure1 was calculated by post processing the data using a simple Perl script.

A similar approach can be used to evaluate CDR block characteristics. Figure 3 illustrates the Jitter transfer curve of the model for a Bang-Bang CDR block implemented using a local VCO and a Bang-Bang Charge Pump in conjunction with a second order RC filter.

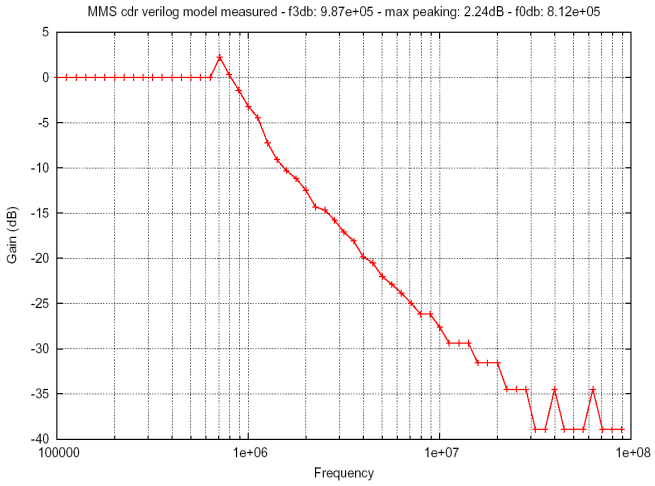

Figure 3. MMS PLL Behavioral Model used in a Spread Spectrum Application

Based on project requirements, accuracy can be optimized for runtime. Figure 4 shows the transfer curves generated for 'case1' shown in Figure 1 while varying the resolution used in the simulation.

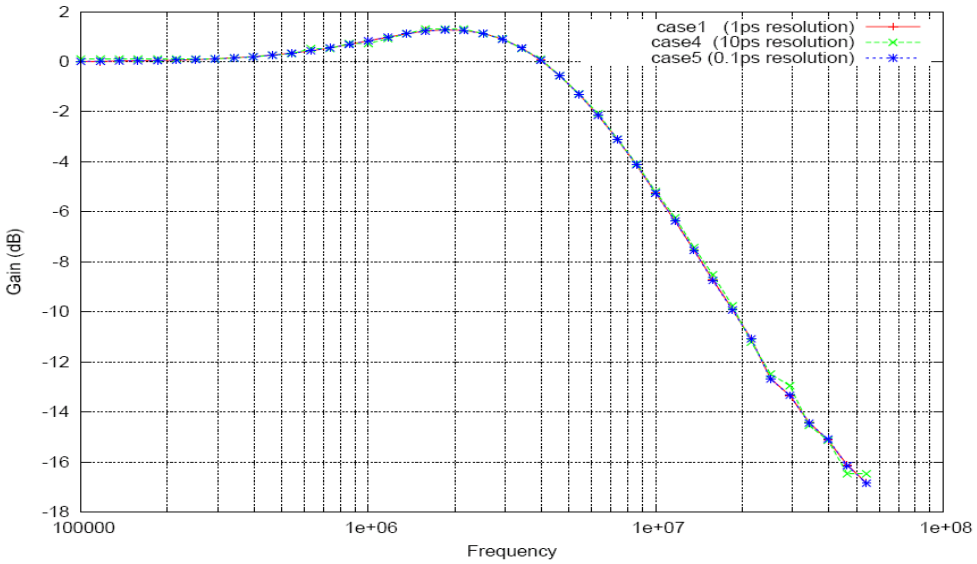

Figure 4. MMS PLL Behavioral Model Results vs. Simulation Resolution

Here, 'case1' was simulated using a 1ps resolution with a runtime of 3hrs 55mins, 'case4' was simulated using a 10ps resolution with a runtime of 3hrs 10mins, and 'case5' was simulated using a 0.1ps resolution with a runtime of 11hrs 45mins. The transfer curves shown were generated based on output from a succession of time domain simulations. Simulation time is dependent on the frequency content of the input phase error frequency content, as it impacts the runtime for each individual simulation.

It should be noted that the simulations were performed on a Linux Laptop using a 1.7GHz Pentium M processor, on an open-source verilog simulator. Using a commercial simulator such as VCS or Verilog-XL would speed up the simulations very significantly (based on public domain benchmarked speed reports) because the simulations times for these scenarios were very lengthy depending on the input phase error frequency content.

Such accurate behavior replication is also very beneficial in architecture development and verification of simulation intensive subsystems such as Spread Spectrum PLLs. Figure 5 shows the output period profile of a PLL model used in a Spread Spectrum clock generation subsystem. The output clock period data can be subsequently post-processed to gather spectral suppression information.

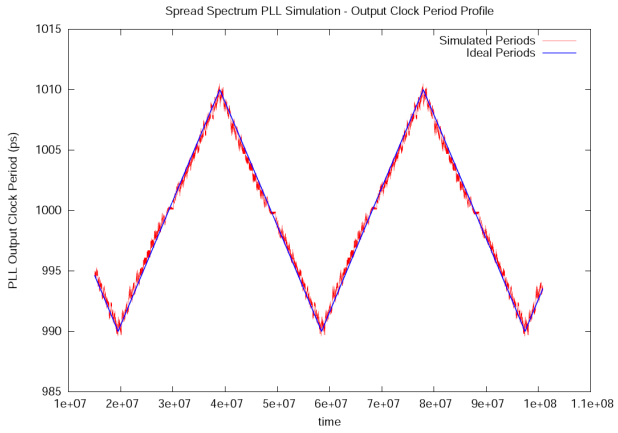

Figure 5. MMS PLL Behavioral Model used in a Spread Spectrum Application

This implementation of an SSC clock generation subsystem illustrates the model capability where a PLL model interacts with a model of a phase interpolator (mixer) and additional digital logic to generate SSC clock output. This capability illustrates the importance in architecture verification of data systems that have a low frequency content. Such systems require long simulations for verification by conventional methods, and the benefits of using such models are more apparent.

In addition to verifying the architectures, the same model can be used to perform chip level simulations by instantiating the blocks??. Since the same model is used, the probability of correct communication between system level interaction during digital Verilog simulation and Analog behavior of such blocks is greatly improved.

Availability and Pricing:

- Analog Component, Generic PLL, SERDES models Available.
- When customer needs exceed MMS Standard Behavioral Model capability, Custom Models and model tailoring are available on request.
- Fixed Price or Price-per-use pricing available on Standard Models.

Contact Mixed Mode Solutions with your model needs Today!: